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Human Body Model (HBM) vs. IEC 61000-4-2

Overview

Many ESD standards such as Human Body Model (HBM), Machine Model (MM), Charged Device Model (CDM) and IEC 61000-4-2 have been developed to test the performance and robustness of electronic devices. Unfortunately, these standards are frequently misunderstood and often used interchangeably. This ultimately results in failures of supposedly protected systems in the consumer's hands. The designer needs to understand the difference between manufacturing environment and end user environment ESD testing.

Most designers are familiar with the classic device level tests that are applied to integrated circuits (IC), but the most common misunderstanding occurs between the human body model and the IEC 61000-4-2 standards. These two standards are designed for very different purposes. Only the stringent IEC 61000-4-2 standard is acceptable to identify real world ESD stress conditions.

The purpose of this brief is to indicate the differences between the HBM and IEC 61000-4-2 Standards and test methods.

There are three important changes in today's systems that have increased ESD vulnerability.

- **Smaller Manufacturing Geometries:** most ICs have decreased to less than 90nm and the voltage and current levels have decreased. ESD damage can occur due to excessive voltage, high current levels or a combination of both. High voltages cause gate oxide punch-through and high current levels cause junction failures and melting of metalized traces. This decrease in geometries has made it very difficult to provide adequate on-chip ESD protection.
- **Reduction of On-Chip Protection:** The Industry Council on ESD Target Specifications announced a move to reduce the standard level of on-chip protection. Their focus is providing adequate protection for manufacturing environments and to maintain protection levels of today's market.
- **The Changing Application Environment:** many laptops, cell-phones (smartphones), MP3 players, digital cameras and other handheld devices that are used in uncontrolled environments require additional ESD protection. In these environments people touch I/O connector pins - such as USB, HDMI, etc. - when plugging or unplugging cables. The devices are subject to constant ESD stress levels when this happens. The portable device can also build up a charge and will discharge when plugged into a grounded device such as a TV or computer. The simple act of walking across a carpet can generate up to 40kV of this level of discharge through a port that can cause latent and permanent defects of so-called protected ICs.

Static Voltage Generation at Different Relative Humidity (RH) Levels		
Generation Method	10-25% RH	60-90% RH
<i>Walking across a carpet</i>	35,000 Volts	1,500 Volts
<i>Walking across vinyl tiles</i>	12,000 Volts	250 Volts
<i>Worker at a workbench</i>	6,000 Volts	100 Volts
<i>Poly bag picked up from workbench</i>	20,000 Volts	1,200 Volts
<i>Sitting on chair with urethane foam</i>	18,000 Volts	1,500 Volts

ESD Standards in the Manufacturing Environment

ICs are susceptible to ESD damage. This damage can occur during the process of assembling and mounting the IC onto a PC board, packaging, shipping or in the field. The current methods for rating ICs ESD susceptibility in the manufacturing environment is:

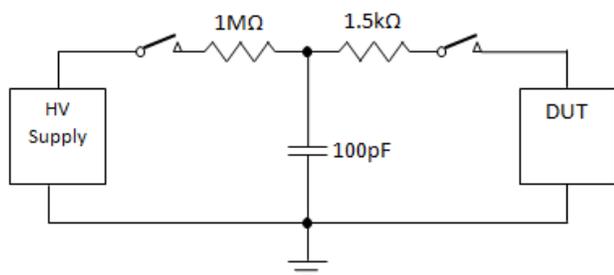
- **HBM:** this standard is intended to simulate a charged person discharging to ground through the circuit under test
- **MM:** this is a simulation of a charged manufacturing machine discharging through the device to ground
- **CDM:** this is a simulation of an IC becoming charged and discharging to a grounded metal surface

The purpose of ESD testing of ICs in the manufacturing environment is very different than system level testing. HBM, MM and CDM are intended to ensure the IC survives the manufacturing process. Most manufacturers of ICs provide just enough ESD protection to survive being assembled into a system. Processes such as packaging, shipping, placement and soldering are all performed in a controlled ESD environment which limits the level of ESD stress to which the device is exposed to. HBM is usually sufficient for controlled environments but it is inadequate for system level testing. The system level testing required is the IEC 61000-4-2.

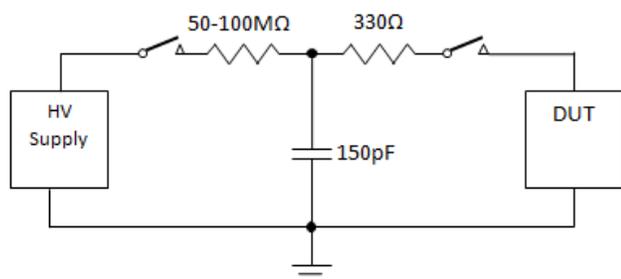
“There are three important changes in today's systems that have increased ESD vulnerability.”

IEC 61000-4-2. The Standard for System Level ESD Testing

The IEC standard replicates a charged person discharging into a system in an uncontrolled environment. This is to ensure the system will remain operational in an end user environment where no ESD stress precautions are taken.



Simulation circuit of HBM, MIL-STD-883



Simulation circuit of IEC6100-4-2

There are four levels of the IEC 61000-4-2 and two test methodologies. Contact Discharge is applying the ESD gun directly to the pin of the device under test. Where touching of the actual pin is not possible then Air Discharge is used. The ESD gun is brought close to the pin until there is a discharge to the pin. The standard is defined so that each level is considered equivalent. A level 4 contact discharge of 8kV is equal to a 15kV Air Discharge.

IEC 61000-4-2 Levels

Contact Discharge		Air Discharge	
Level	Test Voltage kV	Level	Test Voltage kV
1	2	1	2
2	4	2	4
3	6	3	8
4	8	4	15
X <small>Note 1</small>	Special	X <small>Note 1</small>	Special

1. X is an open level. This must be specified in the dedicated equipment specification. Special test equipment may be required.

HBM vs. IEC 61000-4-2

There are several differences between the two standards. The most important differences are:

- The amount of current released during a strike
- The rise time of the voltage strike
- The number of voltage strikes repeated in the test

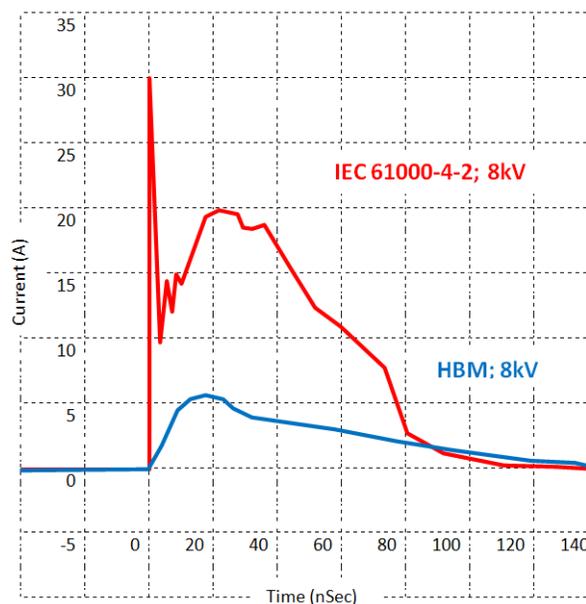
The Amount of Current Released During a Strike

Applied Voltage (kV)	Peak Current (A) Human Body Model	Peak Current (A) IEC 61000-4-2
2	1.33	7.5
4	2.67	15.0
6	4.00	22.5
8	5.33	30.0
10	6.67	37.5

The difference in current is critical to whether the ASIC will survive the ESD strike. It is very possible that an ASIC that has 8kV of HBM can be destroyed by a IEC 61000-4-2 level-1 (2kV) strike. The design engineer should not rely on HBM standards to determine if their application will survive real world ESD strikes when passed on to the end user environment.

The Rise Time of the Voltage Strike

The difference between the two standards is the rise time of the voltage strike. The HBM specifies a rise time of 25nsec. The IEC 61000 has a rise time of less than 1nsec and dissipates most of its energy within the first 30nsec. If it takes 25nsec to respond the device rating using the HBM specification can be destroyed before its protection circuits are even activated (see waveshape below).



The HBM specifications call for a single positive and a single negative strike to be tested. Whereas the IEC 61000 standard requires a minimum of 3 positive and 3 negative strikes. The industry standard is 10 positive and 10 negative strikes. In the HBM it is possible to survive the first strike but fail on subsequent strikes due to damage sustained in the first strike. End user applications will be subjected to many ESD strikes over their lifetime.

Beware of misleading marketing specifications where vendors are increasing their “integrated ESD” rating and confusing system designers by advising that their ICs do not require external ESD protection.

All devices that comply with IEC 61000-4-2 standard will indicate it on their data sheets. Devices that do not state this will normally be tested to HBM or other non IEC 61000-4-2 standards.